501.23549CC5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Y. YAMAGUCHI et al.

Serial No.: Not Yet Assigned

Filed: On Even Date

For: SEMICONDUCTOR MEMORY DEVICE

Group: 2511

Examiner: J. Popek

PRELIMINARY AMENDMENT

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

June 6, 1994

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please add the following new claims:

-- 18. 5 In an address multiplex dynamic RAM having a plurality of memory cells and a plurality of operational modes, a circuit arrangement comprising:

a first external terminal for receiving a row address strobe signal;

a second external terminal for receiving a column address strobe signal;

a third external terminal for receiving a write enable signal;